WHAT IS CLAIMED IS

1. A semiconductor memory device, comprising:

a plurality of input/output terminals;

a memory cell array which are divided into blocks respectively corresponding to said input/output terminals such that only one of the blocks corresponds to a given one of said input/output terminals;

sense amplifiers, which are connected to the blocks at a side thereof, and amplify data of said memory cell array;

switches which are respectively connected to said sense amplifiers; and

signal lines, which connect said sense amplifiers to a corresponding one of said input/output terminals via the switches.

2. The semiconductor memory device as claimed in claim 1, wherein each of the blocks is divided into a plurality of pages, and a selected one of said switches is made conductive in response to an input address so as to select data of a corresponding page to be output from said semiconductor memory device.

3. The semiconductor memory device as

claimed in claim 1, wherein said memory cell array includes flash memory cells.

4. The semiconductor memory device as claimed in claim 3, wherein data of said memory cell array is erased by one unit of erasure, wherein more than one of said blocks are put together to form the unit of erasure.

5. A semiconductor memory device which allows data of a plurality of pages to be read from a memory cell array and stored in sense amplifiers, and allows data of a selected page to be read from the sense amplifiers and output to an exterior of said semiconductor memory device, comprising:

memory cell areas storing data to be input from and output to one common input/output terminal, said memory cell areas respectively corresponding to the plurality of pages and provided adjacent to each other, wherein the sense amplifiers corresponding to said memory cell areas are arranged adjacent to each other; and

signal lines which connect the sense amplifiers corresponding to said memory cell areas to the common input/output terminal.

6. The semiconductor memory device as claimed in claim 5, wherein the memory cell array

includes flash memory cells.

7. The semiconductor memory device as claimed in claim 6, wherein data of said memory cell array is erased by one unit of erasure, wherein the unit of erasure is formed by putting together the memory cell areas for a plurality of input/output terminals.

8. A semiconductor memory device which allows data of a plurality of pages to be read from a memory cell array and stored in sense amplifiers, and allows data of a selected page to be read from the sense amplifiers and output to an exterior of said semiconductor memory device, comprising memory cell areas storing data to be input from and output to one common input/output terminal, said memory cell areas respectively corresponding to the plurality of pages and provided adjacent to each other.

9. A semiconductor memory device which allows data of a plurality of pages to be read from a memory cell array and stored in sense amplifiers, and allows data of a selected page to be read from the sense amplifiers and output to an exterior of said semiconductor memory device, comprising signal lines which connect one common input/output terminal

to the sense amplifiers corresponding to the one common input/output terminal, wherein the sense amplifiers corresponding to the one common input/output terminal are arranged adjacent to each other.

10. A semiconductor memory device, comprising:

an electrically rewritable nonvolatile memory cell array which include a plurality of I/O portions, which are grouped into a plurality of I/O sets;

word lines provided separately for respective ones of the I/O sets; and

word-line drivers provided separately for the respective ones of the I/O sets, wherein the word lines are activated in all the I/O sets during a read operation, and are activated in at least one but not all of the I/O sets during a write operation.

11. The semiconductor memory device as claimed in claim 10, wherein the I/O sets are programmed one after another until all the I/O sets are programmed.

12. The semiconductor memory device as claimed in claim 12, further comprising a write control circuit, which controls a sequence of

programming the I/O sets one after another.